Multiple-Chip Module Design Optimizations Using A Novel Layout Parameterization Technique

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Abstract — **A novel layout parameterization technique for multi-chip module design optimizations is presented. This technique is based on a quasi-static method of moments and multi-dimensional interpolation, which can reduce a 12-minute electromagnetic layout simulation to 5.3 seconds. Excellent CDMA power amplifier (PA) module performance is achieved based on this technique.**

INTRODUCTION

With the advancements of technologies, communication systems are operating at high frequency and speed. Over the past decade, electromagnetic (EM) simulations have been widely applied for the design and verification of layout interconnects and passive circuitry in radio frequency (RF) and microwave (MW) circuit applications. The earliest direct electromagnetic optimizations were presented in [1], that allow design specifications to be reached with full EM accuracy by automatically adjusting physical layout variations in the design. An integrated EM optimization with nonlinear Harmonic Balance simulation is presented in [2], which enables the full optimization of the physical layout in conjunction with non-linear circuit performance. However, the full-wave simulations employed are accurate but time consuming, which limits their applications for optimizing simple structures.

In [3], the quasi-static method of moments (MoM) was presented. Compared with the conventional MoM, the technique significantly reduces the required computational time for non-radiating structures. This feature allows the application of EM simulations for complicated circuit applications to be made rapidly. Based on [3], an integrated EM/circuit design method for complex microwave and millimeter wave IC applications was presented in [4]. Even with the advancements of [3] and [4], it is impractical to use a high-speed EM simulator to model the effects of each layout adjustment in a complicated RF/MW IC and module design, because of time constraints. In this paper, a novel layout parameterization technique is presented. This technique is based on a linear multi-dimensional interpolation of S-parameters. When an EM database is constructed, this technique enables EM/circuit co-simulations and co-optimizations without re-running any EM simulations. With this technique, a 10-12 minute long EM simulation can be achieved in 5.3 second. In addition, techniques for accuracy improvements of EM modeling have been developed and are also presented. An optimization example of an IS-95 CDMA multi-chip module, having the similar complexity as Fig. 1, is presented.

II. THEORY OF LAYOUT PARAMETERIZATION AND S-PARAMETER INTERPOLATION

For this approach, a systematic layout design optimization can be achieved with layout parameterizations and methodical adjustments of the layout parameters. To begin the theoretical development, a circuit of interest, such as the filter in Fig. 2, is parameterized in a one-dimensional parameter L. Tuning of this filter for optimization can be done with the variation of L.

While a layout component is parameterized with N parameters (p_1, p_2, ..., p_N), each set of parameter values represents a sample point $\mathbf{P}$ in the N-dimensional parameter space. To implement this technique, a model database is constructed to store the S-parameter model $S(\mathbf{P})$ generated by the electromagnetic simulator for each sample of the selected set.

Consider a set of M+1 sample points $\{\mathbf{P}^{(0)}, \mathbf{P}^{(1)}, ..., \mathbf{P}^{(M)}\}$ with $1 \le M \le N$ and $M+1 > N$ for which a model has been generated for a specified sample range. Provided that the set of M difference vectors $\{\mathbf{P}^{(1)}-\mathbf{P}^{(0)}, ..., \mathbf{P}^{(M)}-\mathbf{P}^{(0)}\}$ is linear independent, they span an M-dimensional subspace in the N-dimensional parameter space. Hence, each point in the subspace can be uniquely represented as a linear combination by its subspace coordinates (r_1, ..., r_M):

$$\mathbf{P} = \mathbf{P}^{(0)} + r_1(\mathbf{P}^{(1)} - \mathbf{P}^{(0)}) + ... + r_M(\mathbf{P}^{(M)} - \mathbf{P}^{(0)})$$

By introducing the extra coordinate r_0, this can be rewritten as:

$$\mathbf{P} = \sum_{j=0}^{M} r_j \mathbf{P}^{(j)} \qquad (1)$$

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with

$$r_0 = 1 - \sum_{j=1}^{M} r_j \tag{2}$$

The S-parameter model for the sample point **P** is obtained by the M-dimensional linear interpolation (3) from the known S-parameter models in the sample points $\mathbf{P}^{(j)}$ where

$$S(\mathbf{P}) = \sum_{j=0}^{M} r_j S(\mathbf{P}^{(j)}) \tag{3}$$

When the sample **P** is inside the cell build by the set of M difference vectors $\{\mathbf{P}^{(1)}-\mathbf{P}^{(0)}, ..., \mathbf{P}^{(M)}-\mathbf{P}^{(0)}\}$ and the sample **P** is close to the M+1 sample points $\{\mathbf{P}^{(0)}, \mathbf{P}^{(1)}, ..., \mathbf{P}^{(M)}\}$, equation (3) provides an accurate approximation. Two conditions need to be satisfied for accurate interpolations.

The first condition is

$$0 \le r_j \le 1 \tag{4}$$

The second condition requires a distance measurement between **P** and each sample $\mathbf{P}^{(j)}$. A normalized distance parameter is introduced as follows:

$$L_1(\mathbf{P}, \mathbf{P}^{(j)}) = \sum_{k=1}^{N} \left| \frac{p_k - p_k^{(j)}}{\Delta p_k} \right| \tag{5}$$

The normalization for each parameter p_k is with respect to a selected interpolation delta Δp_k. The sample **P** is considered to be close to the sample point $\mathbf{P}^{(j)}$ when $L1 < N$.

For a 2-dimensional parameter problem (N=2), the multi-dimensional linear interpolation (3) reduces to the linear interpolation over a triangle for M=2 (Fig. 3).

Based on equations (1) to (5), the layout parameterization and S-parameter interpolation techniques can be developed. Thus, using the same simulation techniques presented in [4], circuit and EM simulations were done with Agilent Advanced Design System (ADS) and Agilent Momentum RF, respectively, to implement this design optimization technique for the example of this study. Custom programs were constructed to link both the circuit and electromagnetic simulators, which allow the layout/circuit co-simulations, co-optimizations, and the S-parameter interpolation based on available EM models.

III. Accuracy Improvements

In this section, three accuracy improvement techniques for module modeling are presented.

A. Physical Parameter Extractions

The traces on most RF module boards have long electrical lengths with respect to the guided wavelength. It is insufficient to validate EM models with measured S-parameter for such lines. A slight difference in S-parameters can result from two different physical models. Better validations can be achieved with the comparisons of the extracted transmission line parameters [5].

In Fig. 4, the simulated and measured extracted physical parameters of a 280-mil transmission line on a 4-layer laminated board are compared. Excellent agreements are found between the measurements and the EM model. In addition to the transmission parameters, the inductive and capacitive couplings of the EM models should also be validated with transmission measurements between two transmission lines with far ends shorted and opened, respectively. With the validation of all the physical parameters, the accuracy of EM model for multi-layer modules can be guaranteed.

B. Modeling of Discrete Components

In RF modules, there are numerous discrete components. An accurate EM/circuit simulation also requires accurate surface mount component models. The characterizations should be made by attaching the devices to a low k insulator slab and measuring the two terminals with a wide pitched ground-signal probe and a vector network analyzer. This method can avoid the undesired parasitic effects from measurement fixtures. The frequency sweep should be done at least up to the first resonance of the device to extract the device parasitic. To reduce measurement errors, model extractions should be done based on numerous samples. Averaging should also be applied to each measurement.

C. Port De-embedding

The required computation time of MoM is correlated with the square of the number of unknowns [4]. The layout of the entire PA load is modeled within 36 minutes with a 450 MHz workstation. If the layout is characterized with two smaller cascaded models for simulation, the required time for each model is 10-12 minutes. An appropriate layout partition technique for this approach can be found in [4]. However, when the partition is close to a layout discontinuity, the abrupt layout change will result in unwanted parasitic effects at high frequency. To reduce errors in the cascade of EM models, the abrupt edges should be simulated with extended continuous lines. The extended line effects can be removed by

$$\overline{S}' = \left[e^{\gamma}\right] \overline{S} \left[e^{\gamma}\right] \tag{6}$$

$[e^{\gamma}]$ is the diagonal matrix, consisting of compensation factors of the embedded line extensions.

IV. Results

The optimization of the filter (Fig. 2) in the MCM PA module using the proposed technique is presented in this

section. The layout was parameterized in one dimension due to the constraint of the available space and the minimum spacing between components of layout design rules. The EM model database was computed with a 2.4-mil resolution. The accuracy of the proposed interpolation technique was validated at L =1, 13, and 25 mil. These locations are selected not to be sample points. The agreement between EM/circuit simulations and interpolation/circuit simulations are shown in Fig. 5. Excellent agreement is observed. The technique reduces the required computational time from 12 minutes to 5.3 seconds. The optimal designs were found with this technique and validated with measurements in Fig. 6. Excellent agreement is observed between the S-parameter interpolations and measurements. This example proves the usefulness of the proposed technique for MCM design. Other parts of the PA load are also optimized with the same EM/circuit co-simulation. The validations of the load impedance at both high power and low power modes are shown in Fig. 7. This optimal load design is also validated with an IS-95 CDMA PA module. The average test results of 96 samples are shown in Table I. The power added efficiency (PAE) at high power (28 dBm) and low power (16 dBm) are 40% and 14%, respectively. These results are a marked improvement from a more typical efficiency performance of 35% and 7% obtained from commercially available CDMA PA modules. The linearity performance is validated with the adjacent channel power rejection (ACPR) measurement. At 885 kHz away from the channel, the measured ACPR is better than -49 dBc for both high and low power modes and across the whole cellular frequency band.

V. Conclusion

In this paper, a novel layout optimization technique is presented and validated. The proposed technique can reduce a 12-minute EM/layout simulation to 5.3 seconds with the same accuracy, effective for complicated layout design optimizations. Techniques for the accuracy improvement of EM/circuit modeling are also presented. The optimization of a complicated MCM PA load is presented and validated. Excellent CDMA PA module performance has been achieved based on this layout optimization technique.

Acknowledgement

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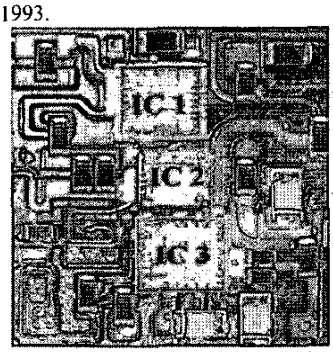


Fig. 1. A generic RF multi-layer multi-chip module.

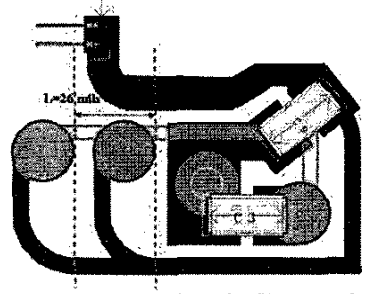


Fig. 2. Layout parameterization of a filter. The left segment L is varied from 0 to 26 mils.

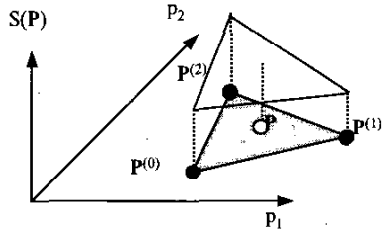


Fig. 3. Multi-dimensional linear interpolation for a 2-parameter problem.

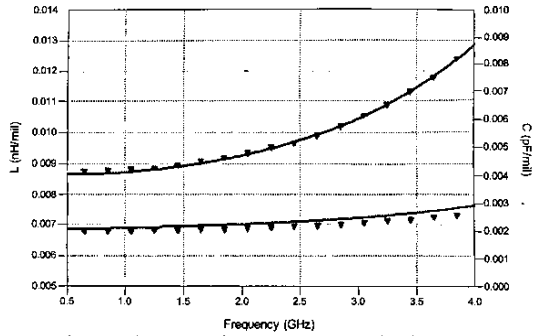
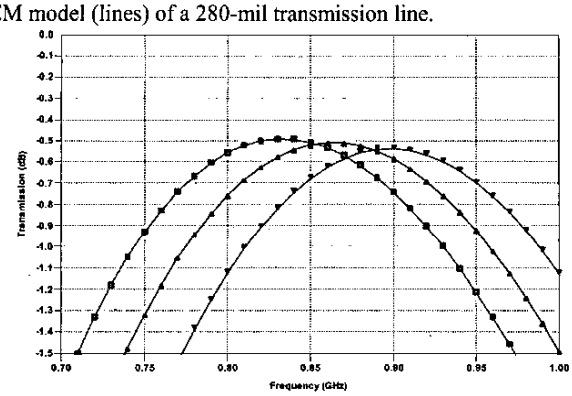
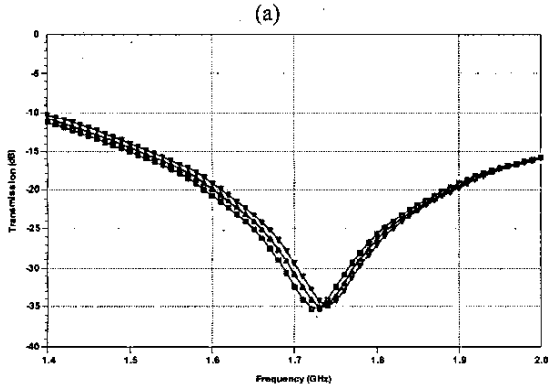


Fig. 4. Comparisons of the extracted inductance and capacitance per unit length from measurements (symbol) and the EM model (lines) of a 280-mil transmission line.



(a)



(b)

Fig. 5. Simulated filter transmission coefficient from the EM models (line) and the S-parameter interpolations (symbol) at (a) fundamental frequencies (b) harmonic frequencies. Traces from the left to the right are L = 1 mil, L = 13 mil, and L = 25 mil.

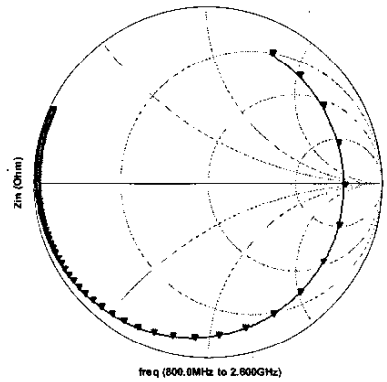
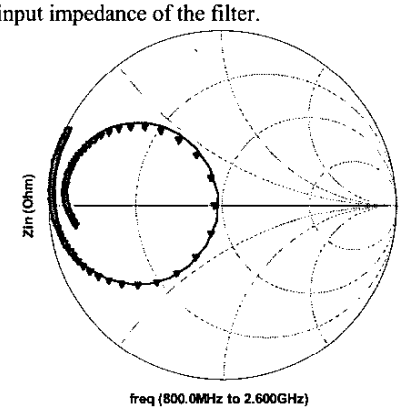
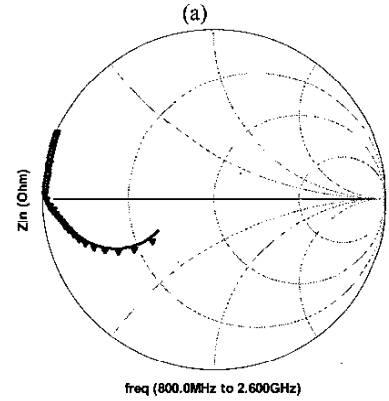


Fig. 6. Comparison of the simulated (line) and the measured (symbol) input impedance of the filter.



(a)



(b)

Fig. 7. Measurements (symbol) versus simulations (line) of the PA load impedance at (a) the high power mode (b) the low power mode.

TABLE I Average test results of 96 cellular band CDMA power amplifiers.

	Low Band		Mid Band		High Band	
Output Power	PAE	ACPR @885 kHz	PAE	ACRP @885 kHz	PAE	ACPR @885 kHz
16 dBm	14.49%	-57.83	13.94%	-56.4	13.70%	-55.77
28 dBm	40.55%	-48.78	40.13%	-50.87	39.88%	-50.46